UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,940	10/15/2003	Kenneth E. Garey	MS-95E069US2	4565

7590 04/17/2006

Intellectual Property Development
Jack J'maey
187 W Orangethorpe Ave
SuiteH
Placentia, CA 92870

EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,940	GAREY, KENNETH E.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Change of Address dated 12/09/2004, Preliminary Amendment dated 3/20/04.

2. Claims 1-20 are presented for examination.

Claim Objections

3. Claim 8 is objected to because of the following informalities: Regarding claim 8, on line 2 of the claim "a" should be removes for purposes of claim processing circuitry. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 10, 12-13, 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Baxter, U.S. Patent 6,058,469.

6. Regarding claim 10, Baxter teaches a signal processor having a programmable logic circuitry that operates on a plurality of data, the signal processor comprising:

a. the programmable logic circuitry (Dynamically Reconfigurable Processing Unit 32, figure 2); and

b. a programmable logic configuration circuitry (reconfiguration logic controls loading the configuration thus loading circuitry, col. 18, lines 21-28) that provides a logic configuration (default configuration, col. 7, lines 11-18) to the programmable logic circuitry.

7. Regarding claim 12, Baxter taught the signal processor according to claim 10, as described above. Baxter further teaches wherein the default configuration is stored in a memory (other configuration data set optimized for implementation of an ISA, col. 12, lines 38-42).

8. Regarding claim 13, Baxter taught the signal processor according to claim 10, as described above. Baxter further teaches wherein the default configuration is stored in a memory (col. 7, lines 11-15).

9. Regarding claim 15, Baxter taught the signal processor according to claim 10, as described above. Baxter further teaches wherein the re-configurable logic circuitry is partitioned into a plurality of areas, each area within the plurality of areas is independently programmable (col. 6, lines 23-25).

10. Regarding claim 16, Baxter a method that provides a logic configuration to a programmable logic circuitry comprising:

a. selecting the logic configuration (reconfiguration interrupts to reference a configuration data set, col. 6, lines 8-22; and reconfiguration logic 104, col. 18, lines 4-27);

b. programming a logic array circuitry using the logic configuration (reconfiguration logic controls loading the configuration thus loading circuitry, col. 18, lines 21-28); and

c. the logic configuration is selected based upon at least one characteristic of a plurality of data (wherein the configuration data corresponds to an ISA, col. 18, lines 20-32).

11. Regarding claim 17, Baxter taught the method according to claim 16, as described above. Baxter further teaches comprising selecting an alternative logic configuration (reconfiguration logic facilitates reconfiguration of DRPU 32, col. 18, lines 4-8).

12. Regarding claim 18, Baxter taught the method according to claim 16, as described above. Baxter further teaches wherein the logic configuration is a default logic configuration (col. 7, lines 11-15).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter, U.S. Patent 6,058,469 in view of Ong, U.S. Patent 5,426,378.

15. Regarding claim 1, Baxter teaches a signal processor having a re-configurable logic circuitry that operates on a plurality of data, the signal processor comprising:

a. a configuration control circuitry that selects at least one logic configuration that is used to program the re-configuration logic circuitry (reconfiguration interrupts reference a configuration data set, col. 6, lines 8-22; and reconfiguration logic 104, col. 18, lines 4-27); and

b. a programmable logic configuration circuitry comprising an active configuration circuitry (default configuration, col. 7, lines 11-18) and a loading configuration circuitry (reconfiguration logic controls loading the configuration thus loading circuitry, col. 18, lines 21-28), and the active configuration circuitry programs the reconfigurable logic circuitry using the at least one logic configuration (change the programming of logic blocks that comprise Reconfigurable Instruction Execution Unit 16, col. 7, lines 3-15).

Baxter does not explicitly disclose wherein the loading configuration circuitry receives at least one additional logic configuration.

Ong teaches a loading configuration circuitry that receives at least one additional logic configuration (a first array for storing one set of configuration data and a second array for storing a second set of configuration data, col. 2, lines 35-47). Ong is similar to that of Baxter in that his invention is directed toward configuring programmable logic. Ong further provides the advantage of reducing the amount of time for re-configuration thereby increasing the number of logic functions that are performed within a programmable logic device with sacrifices in speed and space (col. 2, lines 10-24).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baxter and Ong before them at the time the invention was made, to modify the loading configuration circuity of Baxter to receive at least one additional logic configuration as taught by Ong.

One of ordinary skill in the art would have been motivated to make this modification in order to achieve the advantage of reducing the amount of time for re-configuration thereby

increasing the number of logic functions that are performed within a programmable logic device with sacrifices in speed and space in view of the teaching of Ong.

16. Regarding claim 2, Baxter together with Ong taught the signal processor according to claim 1, as described above. Baxter further teaches wherein the re-configurable logic circuitry further comprises:

a. data memory (data operate unit, col. 6, lines 23-33), a data addressing unit (address operate unit, col. 6, lines 23-33), an arithmetic logic unit, and an instruction decode and sequencing unit (instruction fetch unit, col. 6, lines 23-33); and

b. wherein each of the data memory, the data addressing unit, the arithmetic logic unit and the instruction decode unit and sequencing unit is communicatively coupled to the programmable logic configuration circuitry and is independently programmable unit the programmable configuration circuitry (each of the units are communicatively coupled to the programmable logic configuration unit and are each independently programmable, col. 6, lines 23-25).

17. Regarding claim 4, Baxter together with Ong taught the signal processor according to claim 1, as described above. Baxter further teaches wherein the re-configurable logic circuitry is partitioned into a plurality of areas, each area within the plurality of areas is independently programmable (col. 6, lines 23-25).

18. Regarding claim 5, Baxter together with Ong taught the signal processor according to claim 1, as described above. Baxter further teaches wherein the programmable logic configuration circuitry loads a default logic configuration into the re-configurable logic circuitry (default configuration, col. 7, lines 11-18).

19. Regarding claim 6, Baxter together with Ong taught the signal processor according to claim 1, as described above. Baxter further teaches wherein the default configuration is stored in a memory (col. 7, lines 11-15).

20. Regarding claim 7, Baxter together with Ong taught the signal processor according to claim 1, as described above. Baxter further teaches wherein the default configuration is stored in a memory (other configuration data set optimized for implementation of an ISA, col. 12, lines 38-42).

21. Regarding claim 8, Baxter together with Ong taught the signal processor according to claim 7, as described above. Baxter further teaches wherein the adaptive logic configuration is generated using a processing circuitry (wherein the processing circuitry is reconfiguration logic that loads different configuration, col. 18, lines 20-32).

22. Regarding claim 9, Baxter together with Ong taught the signal processor according to claim 7, as described above. Baxter further teaches comprising data monitoring circuitry that generates the adaptive logic configuration in response to at least one characteristic of the plurality of data (wherein the configuration data corresponds to an ISA, col. 18, lines 20-32).

23. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter, U.S. Patent 6,058,469 and Ong, U.S. Patent 5,426,378 in further view of Young, U.S. Patent 5,933,023.

24. Regarding claim 3, Baxter together with Ong taught the signal processor according to claim 1, as described above. Baxter and Ong do not explicitly disclose wherein the signal processor employs a wide word width to program the re-configurable logic circuitry, the wide word is operable to configure an entirety of the re-configurable logic circuitry.

Young teaches employing a wide word width to program the re-configurable logic circuitry, the wide word is operable to configure an entirety of the re-configurable logic circuitry (dedicated access lines from the FPGA to portion of a RAM are configured to be wide, small or large, col. 2, lines 29-45). Young is in the same field of endeavor as that of Baxter and Ong in that Young is directed toward an FPGA connected to a memory operable to configure logic circuitry. Young further teaches an advantage of allowing efficient connection of RAM blocks.

It would have been obvious to one of ordinary skill in the art, having the teachings of Baxter, Ong and Young before them at the time the invention was made, to modify Baxter to employ a wide word width as taught by Young to program the reconfigurable circuitry within Baxter.

One of ordinary skill in the art would have been motivated to make this modification in order to achieve the advantage of an advantage of allowing efficient connection of RAM blocks.

25. Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter, U.S. Patent 6,058,469 in further view of Young, U.S. Patent 5,933,023.

26. Regarding claim 11, Baxter taught the signal processor according to claim 10, as described above. Baxter does not explicitly disclose wherein the signal processor employs a wide word width to program the re-configurable logic circuitry, the wide word is operable to configure an entirety of the re-configurable logic circuitry.

Young teaches employing a wide word width to program the re-configurable logic circuitry, the wide word is operable to configure an entirety of the re-configurable logic circuitry (dedicated access lines from the FPGA to portion of a RAM are configured to be wide, small or

large, col. 2, lines 29-45). Young is in the same field of endeavor as that of Baxter and Ong in that Young is directed toward an FPGA connected to a memory operable to configure logic circuitry. Young further teaches an advantage of allowing efficient connection of RAM blocks.

It would have been obvious to one of ordinary skill in the art, having the teachings of Baxter and Young before them at the time the invention was made, to modify Baxter to employ a wide word width as taught by Young to program the reconfigurable circuitry within Baxter.

One of ordinary skill in the art would have been motivated to make this modification in order to achieve the advantage of an advantage of allowing efficient connection of RAM blocks.

27. Regarding claim 20, Baxter taught the method according to claim16 as described above. It is further rejected for same reasons as set forth hereinabove in the rejection of claim 11.

28. Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter, U.S. Patent 6,058,469 in further view of Page, "Reconfigurable Processor Architectures".

29. Regarding claim 14, Baxter taught the signal processor according to claim 7, as described above. Baxter does not explicitly disclose wherein the adaptive logic configuration is generated using a processing circuitry.

Page teaches wherein adaptive logic configuration is generated using processing circuitry (on demand usage where the mix of circuitry depends on the actual activity of the system, page 190 left hand column). Page is in the same field of endeavor as that of Baxter in that Page is also directed toward a reconfigurable processor. Page further teaches that using processing circuitry provides the advantage of exploiting different parts of the cost-performance spectrum of implementations (paragraph after section 3.4, page 189, right hand column).

It would have been obvious to on of ordinary skill in the art, having the teachings of Baxter and Page before them at the time the invention was made, to modify Baxter to include wherein the adaptive logic configuration is generated using processing circuitry as taught by Page.

One of ordinary skill in the art would have been motivated to make this modification in order to exploit the cost-performance spectrum of the implementations.

30. Regarding claim 19, Baxter taught the method according to claim 16, as described above. Claim 19 is further rejected for the same reason as set forth in the rejection of claim 14.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,600,845 to Gilson. This patent teaches a signal processor that uses a reconfigurable processor.

U.S. Pat. No. 6,145,020 to Barnett. This patent teaches a signal processor that uses a reconfigurable processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James K. Trujillo
4/02/06

James K. Trujillo
Patent Examiner
Technology Center 2100